Amendment to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application. Claims 1-4, 8-9, and 29-34 are herein canceled without prejudice. Please enter new claims 35-50.

Listing of Claims:

1. – 34. (Canceled)

35. (new) An NMOS transistor comprising:

a dielectric layer above a substrate;

a trench in said dielectric layer, wherein the bottom of said trench is directly above said substrate;

a gate dielectric layer in said trench, wherein a first portion of said gate dielectric layer is adjacent to a first sidewall of said trench, wherein a second portion of said gate dielectric layer is adjacent to a second sidewall of said trench, and wherein a third portion of said gate dielectric layer is on the bottom of said trench;

a gate electrode in said trench, wherein said gate electrode is directly between said first and said second portions of said gate dielectric layer, wherein said gate electrode is comprised of a central portion and a pair of outer portions, wherein said central portion is directly adjacent to said pair of outer portions, wherein the bottom surfaces of said central portion and said pair of outer portions are directly on said third portion of said gate dielectric layer, and wherein the workfunction of

said pair of outer portions if lower than the workfunction of said central portion; and

a pair of n type source/drain regions in said substrate on opposite sides of said pair of outer portions of said gate electrode.

36. (new) The transistor of claim 35 wherein the workfunction of said central portion is between 3.9 to 4.3 eV.

37. (new) The transistor of claim 36 wherein the workfunction of said pair of outer portions is between 1.5 to 3.8 eV.

38. (new) The transistor of claim 35 wherein the workfunction of said pair of outer portions is at least 0.1 eV lower than the workfunction of said central portion.

39. (new) The transistor of claim 35 wherein said pair of outer portions is formed from a material selected from the group consisting of scandium (Sc), magnesium (Mg) and Yttrium (Y).

40. (new) The transistor of claim 39 wherein said central portion comprises a conductive material selected from the group consisting of poly-silicon, titanium, zirconium, hafnium, tantalum, and aluminum.

41. (new) The transistor of claim 35 wherein said central portion of said gate electrode overlaps a portion of said pair of outer portions of said gate electrode.

42. (new) The transistor of claim 41 wherein said pair of outer portions of said gate electrode overlap said pair of n type source/drain regions.

43. (new) A PMOS transistor comprising:

a dielectric layer above a substrate;

a trench in said dielectric layer, wherein the bottom of said trench is directly above said substrate;

a gate dielectric layer in said trench, wherein a first portion of said gate dielectric layer is adjacent to a first sidewall of said trench, wherein a second portion of said gate dielectric layer is adjacent to a second sidewall of said trench, and wherein a third portion of said gate dielectric layer is on the bottom of said trench;

a gate electrode in said trench, wherein said gate electrode is directly between said first and said second portions of said gate dielectric layer, wherein said gate electrode is comprised of a central portion and a pair of outer portions, wherein said central portion is directly adjacent to said pair of outer portions, wherein the bottom surfaces of said central portion and said pair of outer portions are directly on said third portion of said gate dielectric layer, and wherein the workfunction of said pair of outer portions if higher than the workfunction of said central portion; and

a pair of p type source/drain regions in said substrate on opposite sides of said pair of outer portions of said gate electrode

44. (new) The transistor of claim 43 wherein the workfunction of said central portion is between 4.9 to 5.3 eV.

45. (new) The transistor of claim 44 wherein the workfunction of said pair of outer portions is between 5.4 to 6.0 eV.

46. (new) The transistor of claim 43 wherein the workfunction of said pair of outer portions is at least 0.1 eV higher than the workfunction of said central portion.

47. (new) The transistor of claim 43 wherein said pair of outer portions is formed from a material selected from the group consisting of poly-silicon, platinum, and ruthenium nitride (RuN).

48. (new) The transistor of claim 47 wherein said central portion comprises a conductive material selected from the group consisting of ruthenium and palladium.

49. (new) The transistor of claim 43 wherein said central portion of said gate electrode overlaps a portion of said pair of outer portions of said gate electrode.

50. (new) The transistor of claim 49 wherein said pair of outer portions of said gate electrode overlap said pair of p type source/drain regions.